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(54) Electrostatic discharge protection

(57) The invention comprises a system and method for providing electrostatic discharge protection. In one embodiment of the invention, an integrated circuit (10) comprising at least one input element (20) is protected by a protective circuit (40). The protective circuit (40) is operable to protect the integrated circuit (10) from damage due to electrostatic discharge and may be coupled to the input element (20). The protective circuit (40) comprises a lateral NPN transistor (T1) coupled to the input element (20) and operable to activate when the input element voltage exceeds threshold, the threshold greater than or equal to the ordinary operating voltage of circuitry coupled to the input element (20). The protective circuit (40) also may comprise a lateral PNP transistor (T2) coupled to the input element (20) and to the lateral NPN transistor (T1). The lateral PNP transistor (T2) is operable to aid in raising a potential of the base of the lateral NPN transistor (T1). Alternatively, the protective circuit (40) also may use a PMOS transistor (P1), or a PMOS transistor (P1) in combination with the lateral NPN transistor (T1), coupled to the input element (20) and to the lateral NPN transistor (T1). The PMOS transistor (P1) is operable to aid in raising the potential of the base of the lateral NPN transistor (T1).

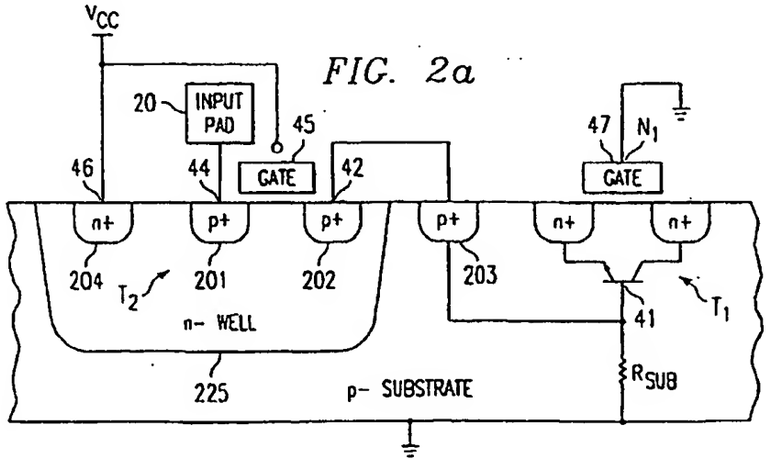

FIG. 2a

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[0001] This invention relates generally to the field of integrated circuits and more particularly to a circuit and method for electrostatic discharge protection of integrated circuits.

[0002] Integrated circuits often employ electrostatic discharge protection to prevent damage to electronic device during an electrostatic discharge event. Such protection may prevent damage from high voltage or current transients, including those that may occur during installation. Metal oxide semiconductor (MOS) integrated circuits are particularly vulnerable to electrostatic discharge because an electrostatic discharge event may melt the silicon or damage gate oxides and/or the short channel devices used in their design. Designing integrated circuits into deep sub-micron scale presents challenges to traditional forms of electrostatic discharge protection.

[0003] One prior approach used for electrostatic discharge protection employs a lateral NPN transistor formed by an n-channel MOSFET (NMOS) or field oxide device between the input and a substrate closely coupled to ground. The device is used to shunt to ground the large transient current caused by an electrostatic discharge event by turning on the lateral NPN when an event occurs. This approach may also utilize a vertical PNP transistor with a collector common to the substrate to trigger forward biasing of the lateral NPN transistor. When placed near the lateral NPN transistor, the vertical PNP transistor may lower the trigger voltage of the lateral NPN by raising the local substrate potential near the base of the lateral NPN transistor.

[0004] This prior approach may not be particularly effective in deep sub-micron products, such as those utilizing silicided CMOS technology. Silicided CMOS products generally have low substrate resistance and often encounter problems with uniform turn-on and even failure of the lateral NPN transistor. This approach may also not be particularly advantageous for mixed signal products, where chip capacitance is normally substantially smaller. In such products, large substrate current injection may be needed to bias the substrate near the lateral NPN transistor. Larger circuit area, not usually available in modern sub-micron designs, may be used to achieve such current injection. Furthermore, the vertical PNP trigger may become de-biased at these chip capacitances. Therefore, a suitably-sized device resistant to debiasing is needed to provide relatively uniform current injection into the substrate, to activate the lateral NPN transistor.

[0005] The invention comprises a system and method for providing electrostatic discharge protection. In one embodiment of the invention, an integrated circuit comprising at least one input element is protected by a protective circuit. The protective circuit is operable to protect the integrated circuit from damage due to electrostatic discharge and may be coupled to the input element. The protective circuit comprises a lateral NPN transistor coupled to the input element and operable to activate when the input element voltage exceeds threshold, the threshold greater than or equal to the ordinary operating voltage of circuitry coupled to the input element, and a lateral PNP transistor coupled to the input element and to the lateral NPN transistor, the lateral PNP transistor being operable to aid in raising a potential of the base of the lateral NPN transistor. Alternatively, the protective circuit also may use a PMOS transistor, or a PMOS transistor in combination with the lateral NPN transistor, coupled to the input element and to the lateral NPN transistor. The PMOS transistor is operable to aid in raising the potential of the base of the lateral NPN transistor.

[0006] The invention provides several important technical advantages. The invention is particularly advantageous in providing uniform turn on of the lateral NPN transistor. The protection circuit is not subject to de-biasing at smaller chip capacitances. Thus, the invention may be used for integrated circuits utilizing silicided CMOS, mixed signal products, or other deep sub-micron or smaller technologies. The invention may also be used with larger technologies. The disclosed protection circuit does not require a large design area in order to provide electrostatic discharge protection, thus potentially conserving valuable circuit space.

[0007] For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in connection with the accompanying drawings in which:

[0008] FIGURE 1 illustrates a schematic diagram of one embodiment of an electrostatic discharge protection circuit utilizing the teachings of the present invention.

[0009] FIGURE 2a illustrates an equivalent circuit cross-section of the embodiment of FIGURE 1.

[0010] FIGURE 2b illustrates a circuit cross-section of a second embodiment of an electrostatic discharge protection circuit utilizing the teachings of the present invention.

[0011] FIGURE 2c illustrates a circuit cross-section of a third embodiment of an electrostatic discharge protection circuit utilizing the teachings of the present invention.

[0012] FIGURE 3 illustrates a cross-section of a fourth embodiment of an electrostatic discharge protection circuit utilizing the teachings of the present invention.

[0013] FIGURE 4 illustrates a top view of the electrostatic discharge protection circuit of FIGURE 3.

[0014] FIGURE 5 illustrates a top view of a fifth embodiment of an electrostatic discharge protection circuit utilizing the teachings of the present invention.

[0015] The present invention and its advantages are best understood by referring to FIGURES 1 through 5 of the drawings, like numerals being used for like and corresponding parts of the various drawings.

[0016] FIGURE 1 illustrates a schematic diagram of

one embodiment of an electrostatic discharge protection circuit. Integrated circuit 10 comprises an input pad 20, a protective circuit 40, and an internal circuit 30. Protective circuit 40 electrically couples input pad 20 to internal circuit 30 and provides protection to internal circuit 30 from damage that may be caused by transient signals resulting from an electrostatic discharge event. Although input pad 20 serves as an input element in this embodiment, any input element could be used without departing from the invention. Although direct connections are illustrated for various elements, many elements may be coupled through other elements without departing from the scope of the invention.

[0017] Protective circuit 40 comprises a lateral NPN transistor TI and a lateral PNP transistor T2, common to a p-type substrate closely coupled to ground. Lateral PNP transistor T2 serves as a trigger. In this embodiment, lateral NPN transistor T1 comprises the drain, source and channel region of an NMOS device N1, while lateral PNP transistor T2 comprises the drain, source and channel region of a PMOS device P1. Lateral NPN transistor T1 and lateral PNP transistor T2 may also be formed using field oxide devices without departing from the scope of the invention.

[0018] Input pad 20 is coupled to internal circuit 30, in this case by a direct connection. Input pad 20 may also be coupled to collector 43 of lateral NPN transistor T1, and to emitter 44 of lateral PNP transistor T2. Emitter 48 of lateral NPN transistor T1 is coupled to ground. Collector 42 of lateral PNP transistor T2 couples to base 41 of lateral NPN transistor T1 at node 100. Node 100 may be coupled to ground through resistance of the substrate, denoted R_{sub}. Gate 47 of NMOS N1 couples to ground through gate resistance R_{gate}. This embodiment employs lateral PNP transistor T2 with both gate 45 of PMOS P1 and base 46 coupled to a reference voltage, denoted V_{cc}. V_{cc} may be any reference voltage, such as one power supply voltage used in integrated circuit 10. The same is true for other references to V_{cc} herein. Other embodiments for lateral PNP transistor T2 may be used without departing from the scope of the invention. Lateral PNP transistor T2 is discussed in further detail in conjunction with FIGURE 2a.

[0019] In operation, protective circuit 40 protects internal circuit 30 by shunting from input pad 20 to ground excess current caused by electrostatic discharge events. Protective circuit 40 operates to limit the current provided to and voltages within internal circuit 30 to operable ranges for devices therein, such as MOSFETS.

[0020] Lateral NPN transistor T1 operates as a high impedance device until an electrostatic discharge event causes a large current or voltage transient at input pad 20. A voltage applied to input pad 20 that causes the voltage between drain 43 and the substrate to reach the junction breakdown voltage, V_{av} activates lateral NPN transistor T1. When lateral NPN transistor T1 is activated, or turned on, by sufficient forward voltage bias V_{av}, current flows through the substrate to ground from collector 43 to emitter 48, creating a low impedance device. It is desirable to reduce V_{av}, because lateral NPN transistor T1 operates more efficiently at voltages lower than V_{av}.

[0021] In this embodiment, NMOS N1 operates to reduce the avalanche voltage, $V_{av,}$ required to turn on lateral NPN transistor T1. Capacitive coupling between input pad 20 and gate 47 of NMOS N1 also operates to reduce the voltage required, $V_{av,}$ to turn on lateral NPN transistor T1. R_{gate} similarly raises the voltage of gate 47 of NMOS N1, thus reducing $V_{av,}$ and providing additional shunt current through NMOS N1 to ground through source 48 of NMOS N1. Reducing avalanche voltage V_{av} reduces the likelihood that lateral NPN transistor T1 will fail. Such failure in protective circuit 40 during an electrostatic discharge event could subject internal circuit 30 to potential damage.

[0022] Lateral PNP transistor T2 may be used to raise the local potential of the substrate near lateral NPN transistor T1, in order to help activate transistor T1. In this embodiment, lateral PNP transistor T2 is used to trigger current injection into the substrate. Lateral PNP transistor T2 injects current from collector 42 to base 41 of lateral NPN transistor T1. This current injection increases the local substrate potential, and thus the voltage of base 41 of lateral NPN transistor T1. This current injection thus triggers the activation of transistor T1 by reducing V_{av}.

[0023] FIGURE 2a illustrates an equivalent circuit cross-section of protective circuit 40 of FIGURE 1. Lateral PNP transistor T2 may be formed by two surface, heavily positively doped (p+) diffusions 201, 202 in an n-well 225 which form emitter 44 and collector 42. The base of lateral PNP transistor T2 is connected to V_{cc} using n+ diffusion 204. In this embodiment, lateral PNP transistor T2 comprises the drain, source and channel regions of PMOS transistor P1, with source 44 at p+ diffusion 201 and drain 42 at p+ diffusion 202. Lateral PNP transistor T2 may also be formed by using a field oxide device, rather than PMOS device P1, without departing from the scope of the invention. Thus, gate 45 of PMOS P1 would be replaced by an isolating oxide that would completely separate the two p+ diffusions 201, 202.

[0024] In this embodiment, emitter 44 couples to input pad 20. Collector 42 couples to base 41 of lateral NPN transistor T1 at p+ diffusion 203. Base 46 of lateral PNP transistor T2 and gate 45 of PMOS P1 are coupled to a power supply voltage V_{cc}. A voltage applied across the base - emitter junction exceeding a threshold voltage of transistor T2 will activate lateral PNP transistor T2, and initiate current flow to collector 42. An embodiment using a PMOS transistor P1 to form lateral PNP transistor T2 will also generate PMOS current from source 44 to drain 42, and may enhance current through collector 42, and thus to base 41 of lateral NPN transistor T1.

[0025] Lateral PNP transistor T2 may also be used in other embodiments without departing from the scope of the invention. For example, in another embodiment il-

lustrated in FIGURE 2b, the source 44 and n-well (also labeled as base 46) of PMOS transistor P1 may be coupled to input pad 20. The drain 42 may be coupled to the base 41 of lateral NPN transistor T1, while the Gate 45 is connected to a reference voltage such as V_{cc}. In such an embodiment, PMOS transistor P1 injects current into base 41 of lateral NPN transistor T1. Here, PMOS transistor P1, may trigger activation of lateral NPN transistor T1 by supplying current to its base region. This embodiment may or may not also employ lateral PNP transistor T2 to aid in the activation of lateral NPN transistor T1.

[0026] Another embodiment may utilize a plurality of lateral NPN transistor T2 or PMOS transistors P1. In yet another embodiment, as illustrated in FIGURE 2c, both source 44 and gate 45 of PMOS P1 may be coupled to input pad 20. Additional current may also be injected into the substrate by forming a vertical PNP transistor V1 near lateral NPN transistor T1. A vertical PNP transistor may be formed by a lateral p-n diode using the substrate as its collector. The lateral p-n diode is coupled to input pad 20 at a p+ diffusion and to supply voltage V_{cc} at an n+ diffusion. Other embodiments of vertical PNP transistors may be used without departing from the scope of the invention. FIGURE 3 illustrates a cross-section of a fourth embodiment of an electrostatic discharge protection circuit utilizing the teachings of the present invention. Protective circuit 40 comprises lateral PNP transistor T2, lateral NPN transistor LT1, and substrate bias ring 60. Substrate bias ring 60 is illustrated and discussed in further detail in conjunction with FIGURE 4. Lateral NPN transistor LT1 comprises a plurality of lateral NPN transistors T1a, T1b, ..., T1n in parallel.

[0027] Substrate bias ring 60 is coupled to both lateral PNP transistor T2 and lateral NPN transistor LT1. As described in conjunction with FIGURES 1 and 2, emitter 44 of lateral PNP transistor T2 couples to input pad 20, and base 46 couples to power supply voltage V_{cc}. Collector 42 of lateral PNP transistor T2 couples to substrate bias ring 60, at p+ diffusion 320.

[0028] Each lateral NPN transistor T1a,..., T1n may be formed by two surface, heavily negatively doped (n+) diffusions. For example, lateral NPN transistor Tla is formed between n+ diffusions 301, 302. In this embodiment, lateral NPN transistor T1a comprises the drain, source and channel regions of NMOS N31, with source 348 at n+ diffusion 301, and drain 343 at n+ diffusion 302. Collector 343 of lateral NPN transistor T1a couples to input pad 20. Emitter 348 couples to ground. Base 341 couples to ground through resistance of the p-type substrate, designated R_{sub}. Collector 42 of lateral PNP transistor T2 and base 341 of lateral NPN transistor T1 are coupled to substrate bias ring 60. Thus, collector 42 of lateral PNP transistor T2 is coupled to each base of transistors T1a, ..., T1n of lateral NPN transistor LT1. Similarly, input pad 20 couples to each collector of transistors T1a,..., T1n of lateral NPN transistor LT1.

[0029] In operation, lateral PNP transistor T2 is used, as discussed in conjunction with FIGURE 1, to raise the local potential of the substrate near lateral NPN transistor LT1, in order to activate each transistor of lateral NPN transistor LT1. Lateral PNP transistor T2 is used in this embodiment to trigger current injection into the substrate.

[0030] Lateral NPN transistor LT1 allows large sizes for lateral NPN transistor T1 without constraining area or distance from input pad 20. Because the plurality of transistors T1a,..., T1n are connected in parallel, proper operation requires turn-on of all transistors T1a,..., T1n before excess current causes failure of one transistor, such as T1a. Because deep sub-micron technologies are subject to low substrate resistance, it is desirable to ensure a relatively uniform distribution of the voltage around each transistor T1a,..., T1n. Relatively uniform injection can thus be applied through all lateral NPN transistors T1a,.... T1n, by raising the substrate potential locally near lateral NPN transistor LT1. Injecting hole current to raise the base voltage of lateral NPN transistor LT1 turns on each transistor T1a,..., T1n without reaching hard avalanche action in the base-collector junction (or drain-substrate junction of each NMOS). Substrate bias ring 60 provides this advantage in this embodiment.

[0031] Lateral PNP transistor T2 injects current from collector 42 to substrate bias ring 60, which is coupled to each base of lateral NPN transistor LT1. Such current injection locally increases the substrate potential near each base of lateral NPN transistor LT1. This current injection into substrate bias ring 60 thus triggers the activation of each lateral NPN transistor T1a, ..., T1n by reducing V_{av}. This method avoids a reliance on avalanche breakdown between each NMOS drain and substrate, which may lead one transistor such as T1a to fail. It thus provides more reliable protection from electrostatic discharge events.

[0032] FIGURE 4 illustrates a top view of the fourth embodiment of an electrostatic discharge protection circuit as illustrated in FIGURE 3. FIGURE 4 clarifies one possible placement of substrate bias ring 60 in protective circuit 40. Protective circuit 40 comprises lateral PNP transistor T2, lateral NPN transistor LT1, and substrate bias ring 60, as shown in FIGURE 3. In this embodiment, lateral NPN transistors T1a,...,Tln comprise the drain, source and channel regions of NMOS N31,..., N3n.

[0033] Substrate bias ring 60 comprises a p+ diffusion area that surrounds lateral NPN transistor LT1. Substrate bias ring 60 may be placed at a distance L from both lateral NPN transistor T1a, and from lateral NPN transistor T1n. Distance L may be small to enhance the substrate bias effect, because there is no SCR structure formed in this protection scheme. Because it may be advantageous to minimize distance L, protective circuit 40 may be designed compactly. For example, one could place substrate bias ring 60 within five microns of lateral NPN transistor LT1.

[0034] FIGURE 5 illustrates a top view of a fifth embodiment of an electrostatic discharge protection circuit utilizing the teachings of the present invention. Protective circuit 500 comprises lateral PNP transistor T2, and a plurality of lateral NPN transistors T5a, ..., T5n comprising the source, drain and channel regions of a plurality of NMOS transistors N51,...,N5n. The plurality of lateral NPN transistors T5a, ..., T5n are connected in parallel. Protective circuit 500 also comprises p+ diffusions 5a, ..., 5n.

[0035] Each of the p+ diffusions 5a, ..., 5n may be coupled to both lateral PNP transistor T2 and the plurality of NPN transistors T2a, ..., T2n. As described in conjunction with FIGURES 3 and 4, emitter 44 of lateral PNP transistor T2 couples to input pad 20, and base 46 couples to power supply voltage V_{cc}. Collector 42 of lateral PNP transistor T2 also coupled to each of the p+ diffusions 5a, ..., 5n.

[0036] P+ diffusions 5a, ..., 5n may be interspersed between each of the plurality of NPN transistors T2a, ..., T2n to raise the local substrate potential near each of the plurality of transistors.

[0037] As described in conjunction with FIGURE 3, the source, drain and channel regions of NMOS transistors N51,...,N5n forms a lateral NPN transistor. For example, a lateral NPN transistor is formed between n+ diffusions 501, 502, with a source at n+ diffusion 301, and drain at n+ diffusion 302. A collector for each lateral NPN transistor couples to input pad 20. An emitter couples to ground. A base couples to ground through resistance of the substrate. Collector 42 of lateral PNP transistor T2 and the base of each lateral NPN transistor are coupled to each of the p+ diffusions 5a, ..., 5n. Similarly, input pad 20 couples to the collector of each lateral NPN transistor.

[0038] In operation, lateral PNP transistor T2 is used, as discussed in conjunction with FIGURE 3, to raise the local potential of the substrate near each of the plurality of NMOS transistors N51,...,N5n, in order to activate each lateral NPN transistor. Lateral NPN transistor T2 is used in this embodiment to trigger current injection into the substrate. In this embodiment, current is injected into each of the p+ diffusions 5a, ..., 5n between each NMOS transistors N51,...,N5n, rather than into substrate bias ring 60 as shown in FIGURES 3 and 4.

[0039] Although the present invention has been described in detail, it should be understood that various changes, substitutions, and alterations can be made hereto without departing from the scope of the invention as defined by the appended claims.

Claims

1. A protective circuit for electrostatic discharge protection of an integrated circuit including:

   a lateral NPN transistor for connection between an element and a voltage-supply terminal of the integrated circuit, capable of diverting electrostatic discharge energy from the element of the integrated circuit when activated and

   a lateral PNP transistor for connection between the element and a reference-voltage terminal of the integrated circuit, so connected to the lateral NPN transistor as to be capable of activating the lateral NPN transistor when the voltage at the element reaches a threshold voltage determined by the reference voltage.

2. An integrated circuit including a protective circuit for electrostatic discharge protection, including:

   a lateral NPN transistor connected between an element and a voltage-supply terminal of the integrated circuit, capable of diverting electrostatic discharge energy from the element of the integrated circuit when activated and

   a lateral PNP transistor, connected between the element and a reference-voltage terminal of the integrated circuit, so connected to the lateral NPN transistor as to be capable of activating the lateral NPN transistor when the voltage at the element reaches a threshold voltage determined by the reference voltage.

3. A circuit as claimed in claim 1 or claim 2, wherein the p-type semiconductor region serving as a collector region of the lateral PNP transistor is connected to the p-type semiconductor region serving as a base region of the lateral NPN transistor.

4. A circuit as claimed in any one of claims 1 to 3, wherein the p-type and n-type semiconductor regions of the lateral PNP transistor serve as the drain, source and channel regions of a p-channel MOSFET, the circuit including a gate electrode for the MOSFET positioned over the n-type region which serves as the channel of the MOSFET.

5. A circuit as claimed in any one of claims 1 to 4, wherein the p-type and n-type semiconductor regions of the lateral NPN transistor serve as the drain, source and channel regions of an n-channel MOSFET, the circuit including a gate electrode for the MOSFET positioned over the p-type region which serves as the channel of the MOSFET.

6. A circuit as claimed in any one of claims 1 to 5, including, additionally, a vertical PNP transistor connected to drive the lateral NPN transistor when connected to the element of the integrated circuit.

7. A circuit as claimed in any one of claims 1 to 6, wherein the lateral NPN transistor is a multiple transistor comprising a plurality of lateral NPN transis-

tors connected in parallel, each transistor being located near a p-type region in a substrate.

8. A circuit as claimed in claim 7, wherein each transistor is located within approximately five microns of a p-type region in the substrate.

9. A circuit as claimed in claim 7 or claim 8, wherein the transistors are surrounded by a substrate biasing area.

10. A circuit as claimed in any one of claims 1 to 6, wherein the lateral NPN transistor is a multiple transistor comprising a plurality of lateral NPN transistors connected in parallel, some of the transistors including a p-type region in the substrate between them.

11. A method for providing electrostatic discharge protection in an integrated circuit, including the steps of:

fabricating a lateral NPN transistor connected between an element and a voltage-supply terminal of the integrated circuit, capable of diverting electrostatic discharge energy from the element of the integrated circuit when activated and

fabricating a lateral PNP transistor, connected between the element and a reference-voltage terminal of the integrated circuit, so connected to the lateral NPN transistor as to be capable of activating the lateral NPN transistor when the voltage at the element reaches a threshold voltage determined by the reference voltage.

12. A method as claimed in claim 12, including the step of fabricating a connection between a p-type region serving as the collector region of the lateral PNP transistor and a p-type region serving as the base region of the lateral NPN transistor.

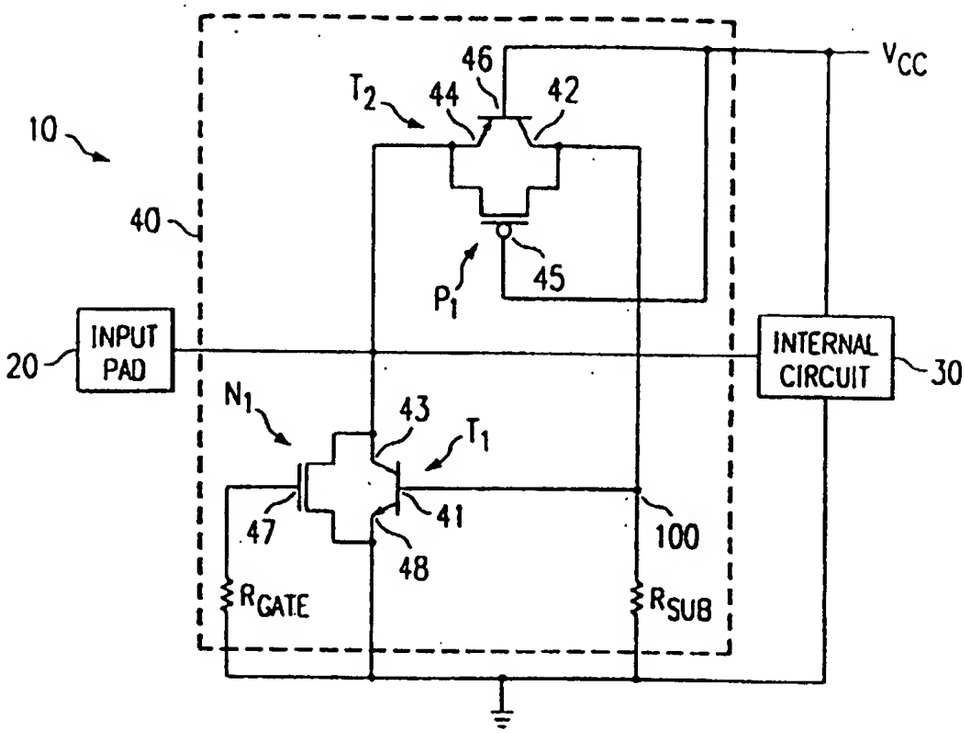
13. a method as claimed in claim 11 or claim 12, including the step of so fabricating a gate electrode over the n-type region of the lateral PNP transistor the p-type and n-type regions of the lateral PNP transistor serve as the drain, source and channel regions of a p-channel MOSFET.

14. A method as claimed in any one of claims 11 to 13, including the step of fabricating a multiple the lateral NPN transistor comprising a plurality of lateral NPN transistors connected in parallel and locating each transistor near a p-type region in a substrate.

15. A method as claimed in claim 14, including the step of locating each transistor within approximately five microns of the p-type region.

16. A method as claimed in claim 14 or claim 15, including the step of surrounding the transistors by a substrate biasing area.

FIG. 1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40
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T_2
44
42
45
P_1
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N_1
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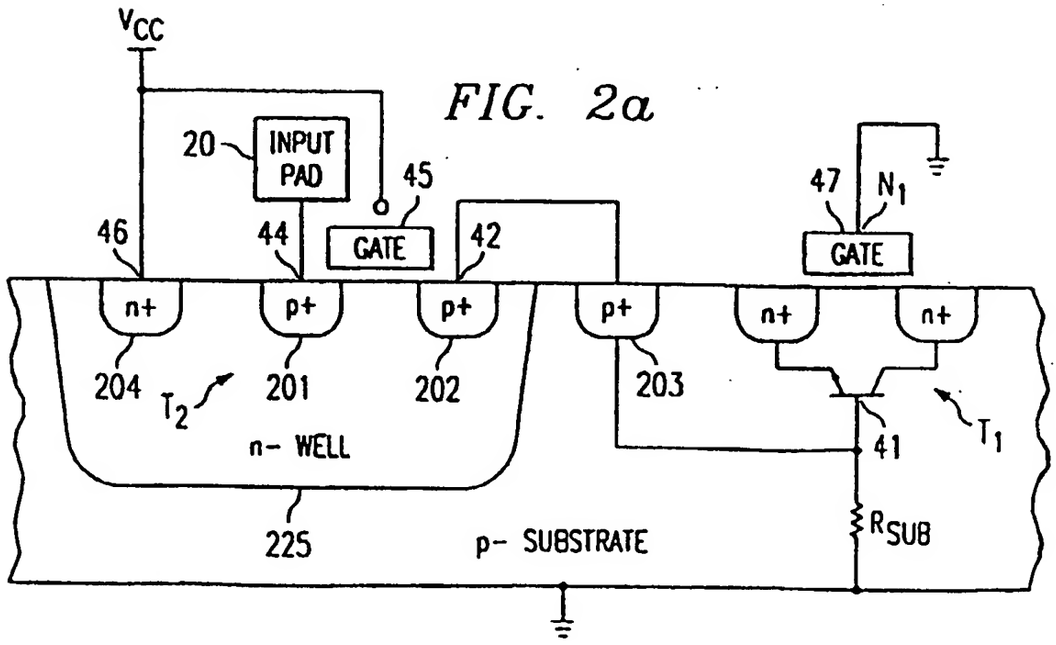
T_1
41
47
48
100
R_{GATE}
R_{SUB}

FIG. 2a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GATE
46
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42
47
N_1
GATE
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p+
p+
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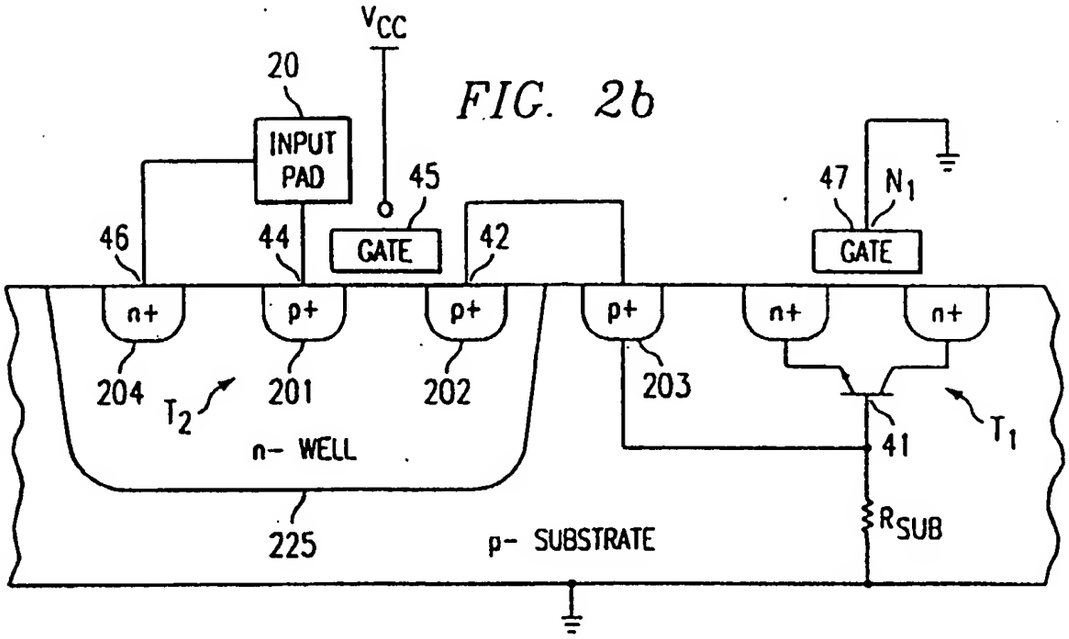
201
202
203
n- WELL
41
T_1
225
p- SUBSTRATE
R_{SUB}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45
GATE
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47
N_1
GATE
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p+
p+
p+
n+
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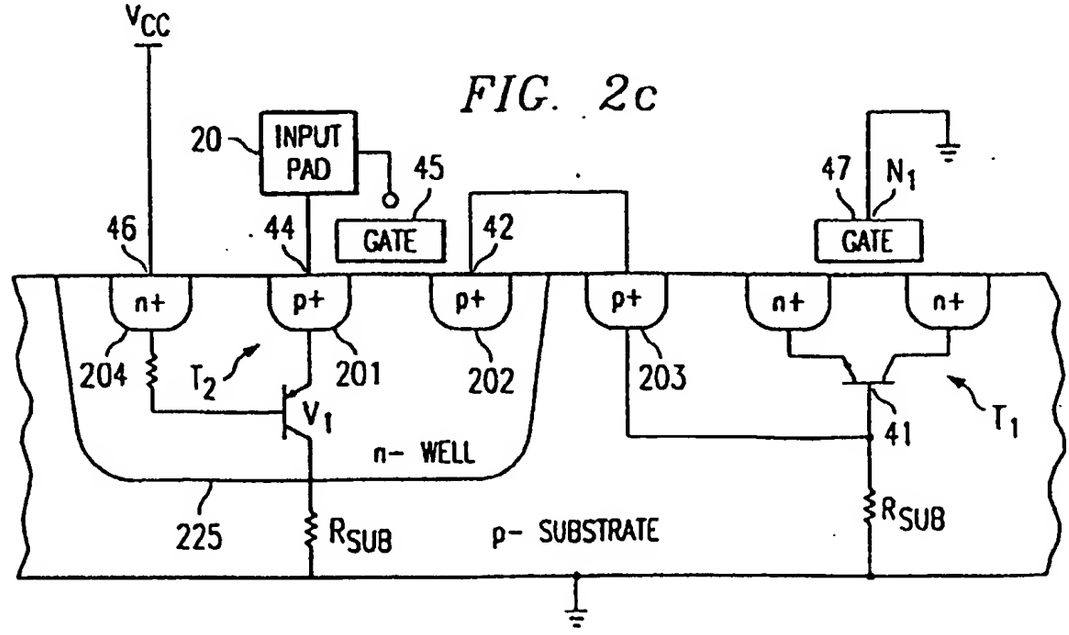
204
T_2
201
202
203
41
T_1
n- WELL
225
p- SUBSTRATE
R_{SUB}

FIG. 2b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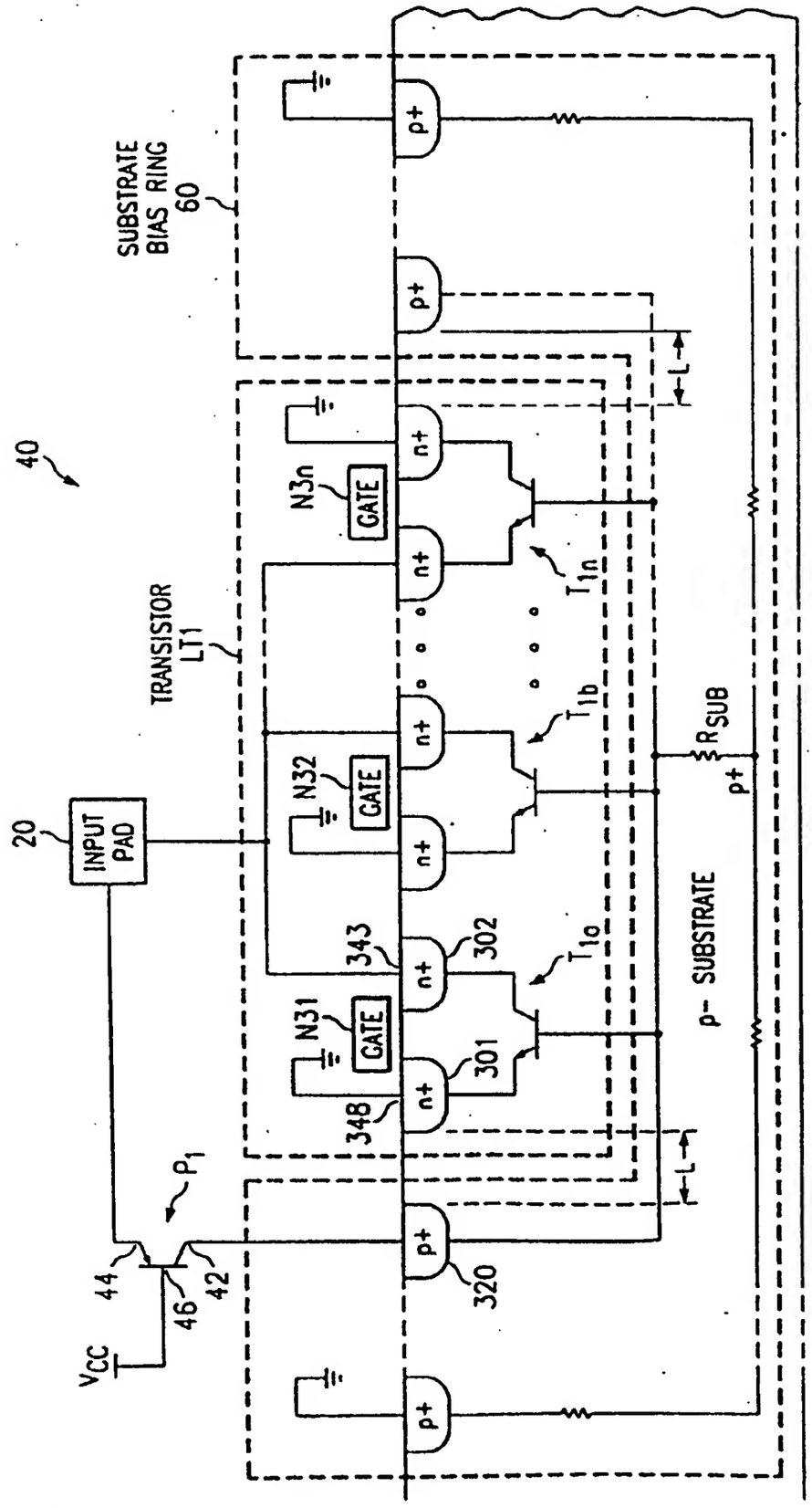
n+
204
T_2
201
202
203
V_1
41
T_1
n- WELL
225
R_{SUB}
p- SUBSTRATE
R_{SUB}

FIG. 2c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SUBSTRATE BIAS RING
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TRANSISTOR LT1
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INPUT PAD
N3n
N32
N31
GATE
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T_{1n}
T_{1b}
T_{1o}
R_{SUB}
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P_1
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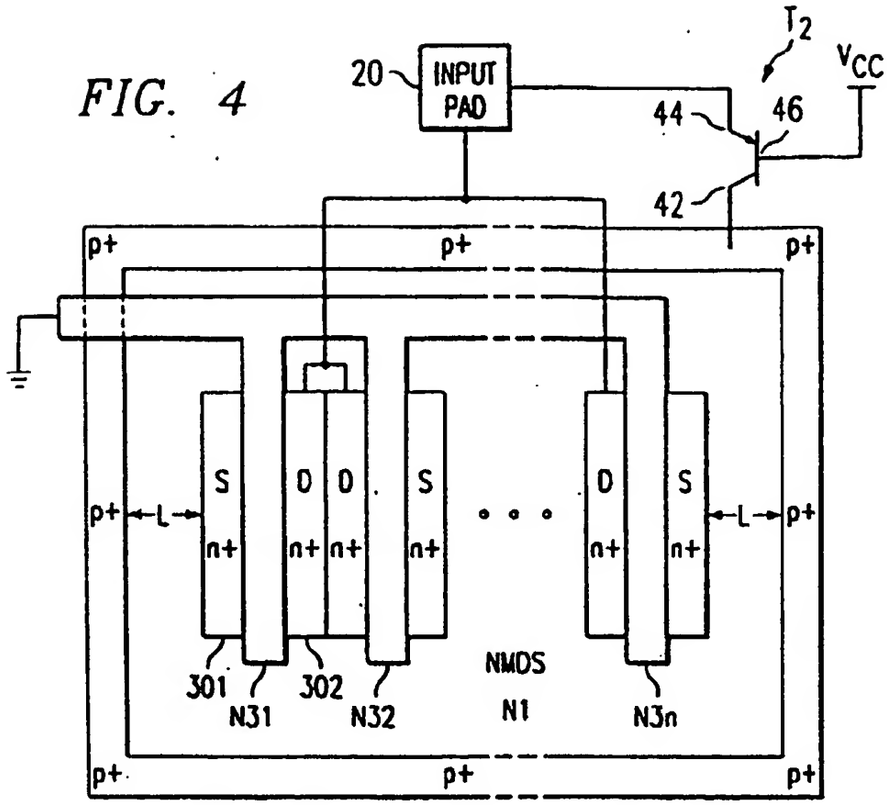
p+

FIG. 3

FIG. 4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INPUT PAD
T2
VCC
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p+
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n+
L
301
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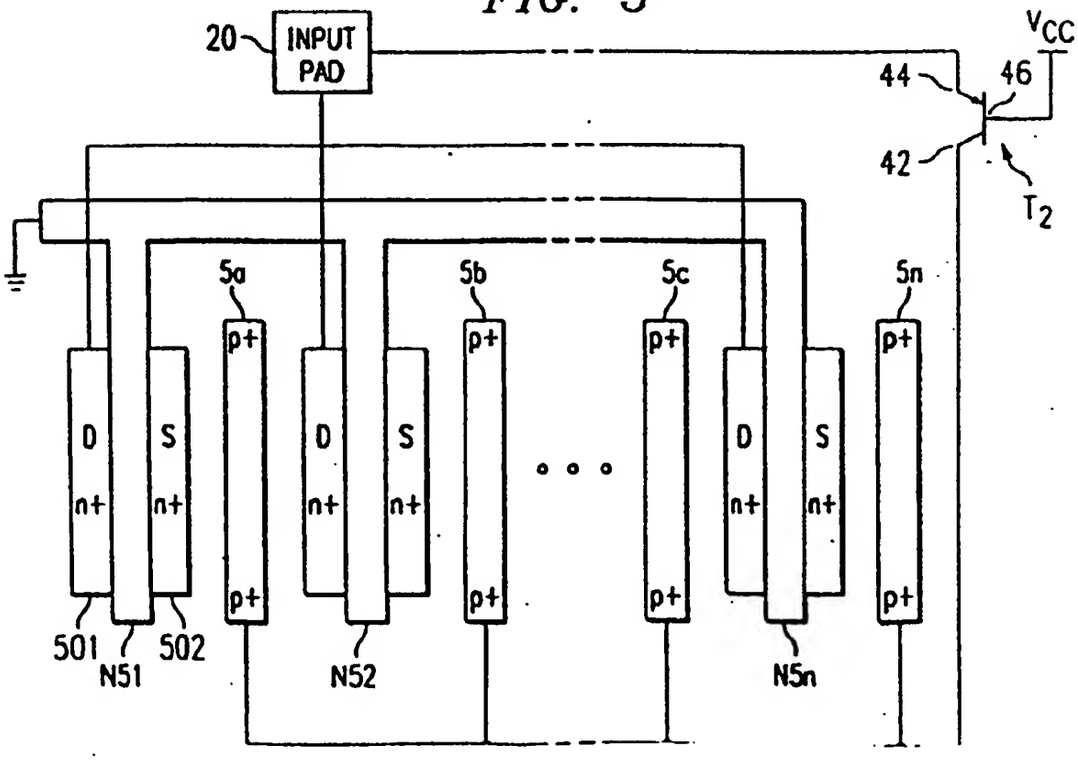
N31
N32
NMOS
N1
N3n

FIG. 5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N51
N52
N5n

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 30 3226

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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Y		7-10, 14-16	
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BERLIN	30 June 2000	Polesello, P

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